On the Optimum Design of Microwave Active Frequency Doublers

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Abstract

A design procedure for the optimum design of microwave active frequency doubler is presented. The proposed methodology is based on a nonlinear mixed analysis / optimisation algorithm giving simultaneuos solution and first-step optimization of the active multiplier. Design charts relying on repeated anaysis / optimizations allow the designer to trade-off between conversion gain, output power and available input power.

Introduction

The increasing demand of a high level of functional integration in many subsystems pushes is actually pushing MMIC designers toward the development of entirely on-chip complex functions. A complete receiver can nowadays be realised onto a single MMIC: the implementation of different functional components with the same technology suggests the usage, wherever possible, of active devices. Active multipliers are therefore key components in this design strategy, allowing both conversion gain, a compact design and compatibility with other subsystems in the same chip. A robust and efficient design methodology is however highly desirable, for an accurate and fast design of the active multiplier and subsequent time-to-market reduction. In this paper a novel design procedure for active microwave frequency doublers is presented: on the basis of a nonlinear analysis / pre-optimisation algorithm, the conversion performances of the active device are investigated and presented to the designer for the necessary trade-off among drive level, output power and conversion gain in the form of design charts. The complete generation of such charts is very fast (comparable to a single complete analysis with commercial simulators) and avoids unnecessary design overheads.

Design assumptions

The major source of frequency generation in active devices is by far the output controlled current source, with the gate biased near pinch-off or in proximity of the gate threshold voltage [1, 2, 3]. Neglecting the second class of operation, which often leads to device degradation due to the presence of current spikes in the input circuit of the device, the present anaysis will focus on the first one, so biasing the device close to pinch-off. With this assumption, the drain bias can be chosen in order to allow the maximum allowable swing of the output voltage [4]. Following such bias conditions, a proper set of harmonic terminations must be selected, maximizing the frequency generation of the device at the selected harmonic. Referring to fig.1, the harmonic termination of major concern are the input source impedance, both at the fundamental and second harmonic (namely $\mathbf{Z}_{s,i}$, i=1,2) and the output load impedances (namely $\mathbf{Z}_{L,i}$, i=1,2). Following intuition and [1-3, 5], both $\mathbf{Z}_{s,2}$ and $\mathbf{Z}_{L,1}$ must be purely reactive, in order to minimize losses and to increase the isolation both of the power source and of the load [5]. Moreover, the input of the device must be conjugately matched at the input frequency

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under large-signal drive to ensure maximum power transfer from the available power source. Conversely, to maximize the output power, a purely resistive load must be presented at the internal controlled current source at the second harmonic *under large-signal drive*: to this purpose, both the input second-harmonic load and the output reactive part of the load can be used.

Analysis method

The assumptions above can be inserted into an analysis/optimization method which automatically imposes the fulfillment of harmonic-balancing equations together with optimum loading both at the fundamental and second harmonic frequencies. The method, already presented in its essential features in [6], is applied to the specific case of frequency multipliers. For this purpose, using a device model obtained via pulsed DC measurements and multibias S-parameters for a medium power GMMT device [7], the following conditions have been imposed within the analysis process, for a given bias point and input drive level: 1) maximum swing of the input voltage at the fundamental, to maximize the output current swing, leading to optimum $X_{L,1}$; 2) maximum power transfer (conjugate matching) at the input frequency at large signal, so determining $Z_{s,1}$; 3) maximum swing of output current and voltage at the second harmonic, leading to optimum reactive part of the load at the second harmonic ($X_{L,2}$). It must be stressed that the above conditions have been inserted in the analysis in the form of equations that are solved together and consistently with the harmonic balance equations. At the end of the analysis, a preoptimized multiplier stage is therefore obtained: in fig. 2 typical waveforms of input voltage, output voltage and current are plotted *vs.* time and a typical dynamic load line is presented in fig.3, superimposed on the device output characteristics. Both plots are obtained for a bias point close to device's pinch-off (Vgg= V, Vdd= V) and for a 15-30 Ghz multiplying stage.

Design methodology

The variables left to the designer to trade-off between drive level, conversion gain and output power are the resistive part of the load ($R_{L,2}$) and the reactive part of the input load ($X_{s,2}$), both at the second harmonic. If the analysis/optimization is repeated sweeping the values of the above variables for different drive levels, the results can be put in the form of design charts of the type shown in fig.4. As it can be clearly noted, the effect of the input terminating reactance at the second harmonic is crucial for the optimum design of high-efficiency multipliers: depending on the drive level selected, It must be stressed that the complete plots have been obtained in a few minutes using a 80486 PC with a nonoptimized code; on the other hand, the results are based on an exact analysis method, having the same accuracy level of standard commercial CAD packages and using a complete nonlinear device model (see fig.1).

Conclusions

A novel procedure for the optimum design of high-efficiency frequency multipliers has been presented. It is based on a full nonlinear analysis/optimization method that consistently analyzes and preoptimizes the multiplying stage, thus giving the possibilty to the designer to fulfill the design specifications utilizing clear and comprehensive design charts.

References

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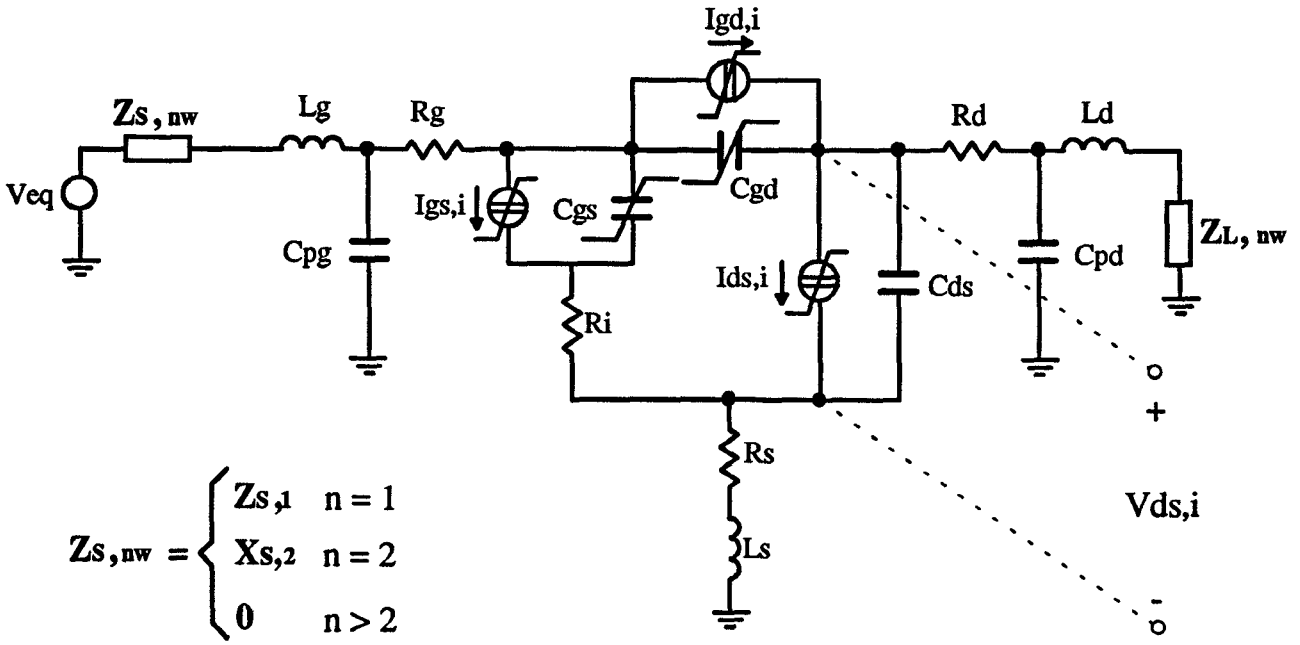

$$Z_{s,nw} = \begin{cases} Z_{s,1} & n = 1 \\ X_{s,2} & n = 2 \\ 0 & n > 2 \end{cases}$$

$$Z_{L,nw} = \begin{cases} X_{L,1} & n = 1 \\ R_{L,2} + jX_{L,2} & n = 2 \\ 0 & n > 2 \end{cases}$$

$$Z_{gen,nw} = \frac{V_{ds,i(nw)}}{I_{ds,i(nw)}} \qquad n=1,2....$$

Fig.1. The equivalent circuit of the nonlinear device with the design quantities indicated

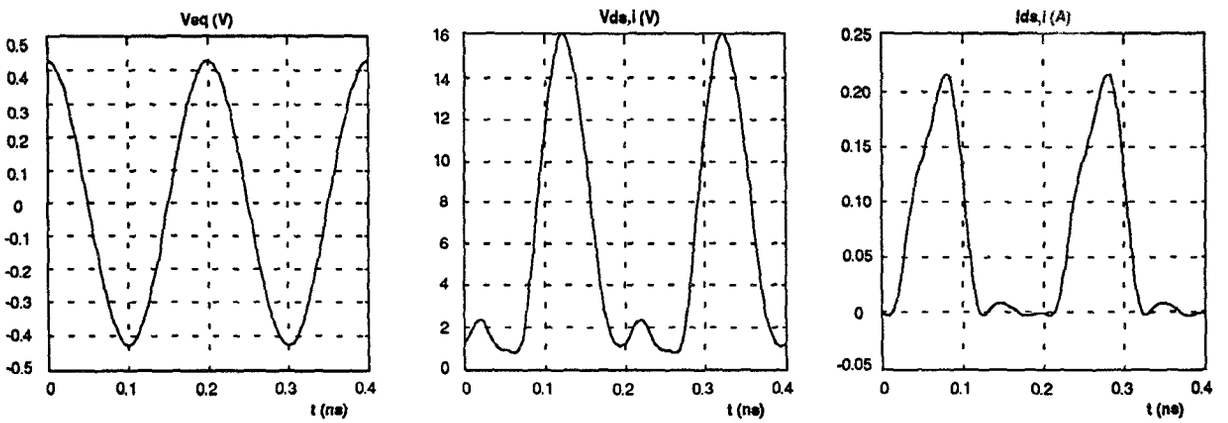

Fig.2. Typical voltages in a multiplying stage

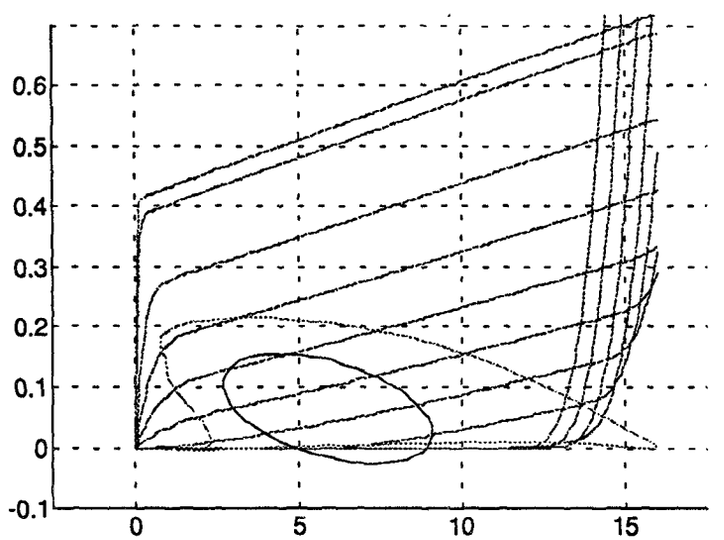

Fig.3. Typical load lines: at the intrinsic and at the load (ellipse)

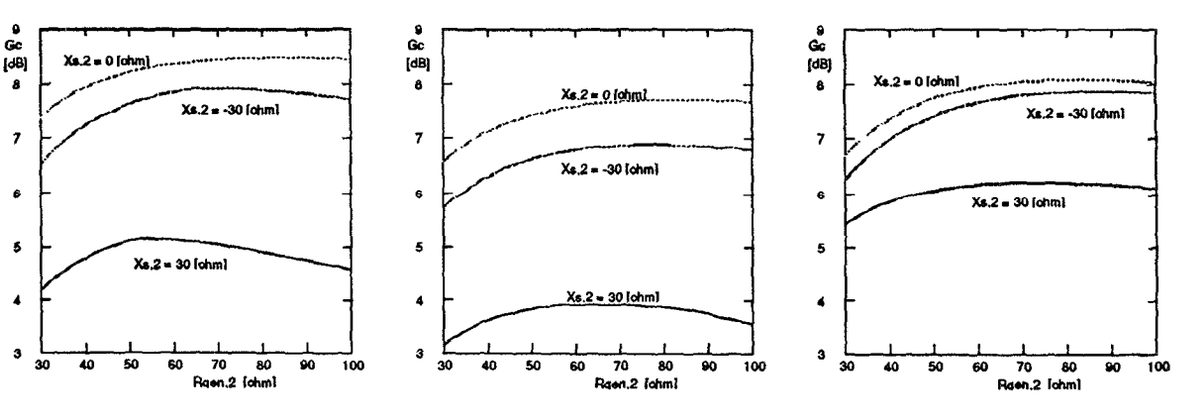

Fig.4. Conversion gains for three different drive levels (6, 8, 10 dBm) and three different values of $X_{s,2}$